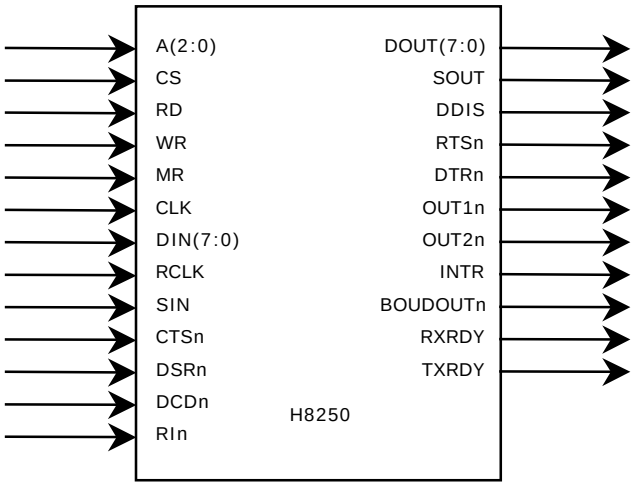
H8250 Megafunction
Universal Asynchronous Receiver/Transmitter

General Description

The H8250 is a standard UART providing 100% software compatibility with the popular Intel 8250 device. It performs serial-to-parallel conversion on data originating from modems or other serial devices, and performs parallel-to-serial conversion on data from a CPU to these devices.

Developed for easy reuse in Altera FPGA applications, the H8250 is available optimized for several device families with competitive utilization and performance characteristics.

Symbol



Applications

- Serial or modem computer interface
- Serial interface within modems and other devices

Features

- Capable of running all existing 8250 software
- Adds or deletes standard asynchronous communication bits (start, stop and parity) to or from the serial data
- Independently controlled transmit, receive, line status and data set interrupts
- Programmable baud generator divides any input clock by 1 to (2^{16} - 1) and generates the 16 x clock
- Independent receiver clock input
- Modem control functions (CTSn, RTSn, DSRn, DTRn, RIn, and DCDn)
- Fully programmable serial interface characteristics:
  - 5, 6, 7, or 8 bit characters
  - Even, odd, or no-parity bit generation and detection
  - 1, 1½, or 2 stop bit generation
  - Baud generation
- False start bit detection
- Complete status register
- Internal diagnostic capabilities: loopback controls for communications link fault isolation
- Full prioritized interrupt system controls

Pin Description

Name	Type	Polarity	Description
MR	In	High	Master Reset (Asynchronous)
CLK	In	-	Master clock (Should be Global Signal)
RCLK	In	-	Receiver clock (Recommended as Global Signal)
RD	In	High	Read control
WR	In	Falling	Write control (Recommended as Global Signal)
CS	In	High	Chip Select
DIN[7:0]	In	-	Data Input Bus
CTSn	In	Low	Clear-to -Send
DSRn	In	Low	Data Set Ready
DCDn	In	Low	Data Carrier Detect
SIN	In	-	Serial Input Data
RIn	In	Low	Ring Indicator
A[2:0]	In	-	Register Select
DOUT[7:0]	Out	-	Data Output Bus
SOUT	Out	-	Serial Output Data
DDIS	Out	High	Driver Disable
RTSn	Out	Low	Request-to-Send
DTRn	Out	Low	Data Terminal Ready
OUT1n	Out	Low	Output 1
OUT2n	Out	Low	Output 2
INTR	Out	High	Interrupt pending
BAUDOUTn	Out	Low	Baud Out
RXRDY	Out	Low	Receiver Ready to Receive Transmissions
TXRDY	Out	Low	Transmitter Ready to Transmit Data

Register Description

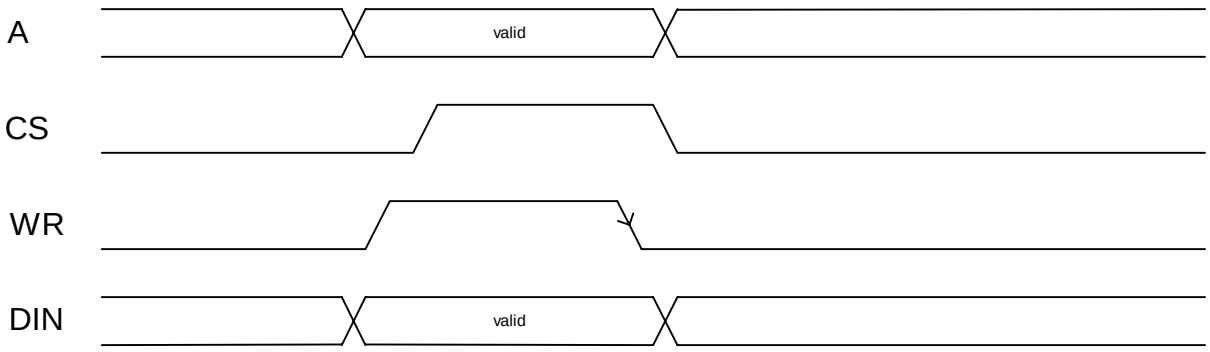
A(2:0)	Divisor * Latch Access Bit	Name	Symbol	Default (reset) value	No. bits	Read/ Write
0	0	Receiver Buffer Register	RBR	XX	8	R
0	0	Transmitter Holding Register	THR	XX	8	W
0	1	Divisor Latch (LSB)	DLR	01h	8	R/W
1	1	Divisor Latch (MSB)	DMR	00h	8	R/W
1	0	Interrupt Enable Register	IER	00h	8	R/W
2	X	Interrupt Identification Register	IIR	01h	8	R
3	X	Line Control Register	LCR	00h	8	R/W
4	X	Modem Control Register	MCR	00h	8	R/W
5	X	Line Status Register	LSR	60h	8	R
6	X	Modem Status Register	MSR	00h	8	R
7	X	Scratch Register	SR	00h	8	R/W

*DLAB is the MSB of the Line Control Register

Switching Characteristics

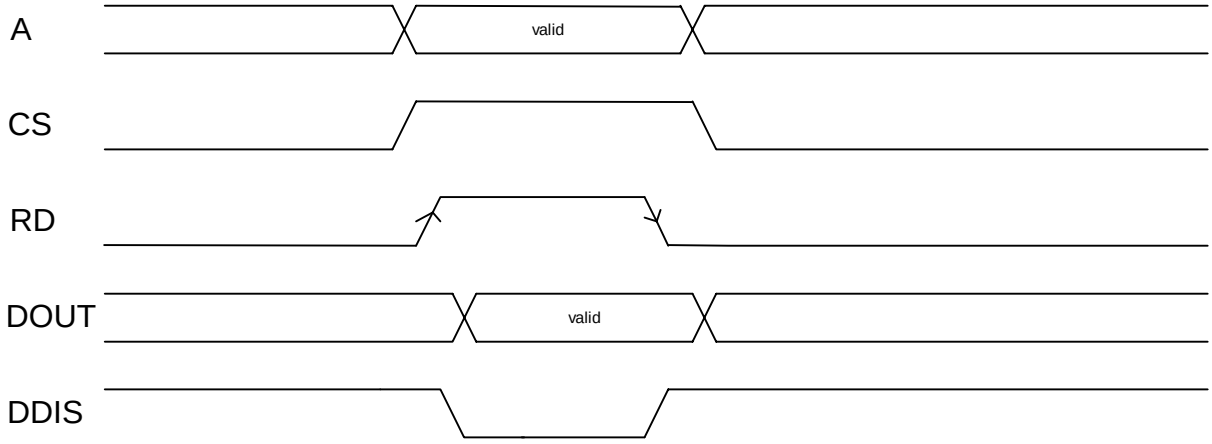
Register Write

The Address (A) and Chip Select (CS) signals are not latched and therefore must be valid throughout the write process. Writing is done at the falling edge of the WR signal.



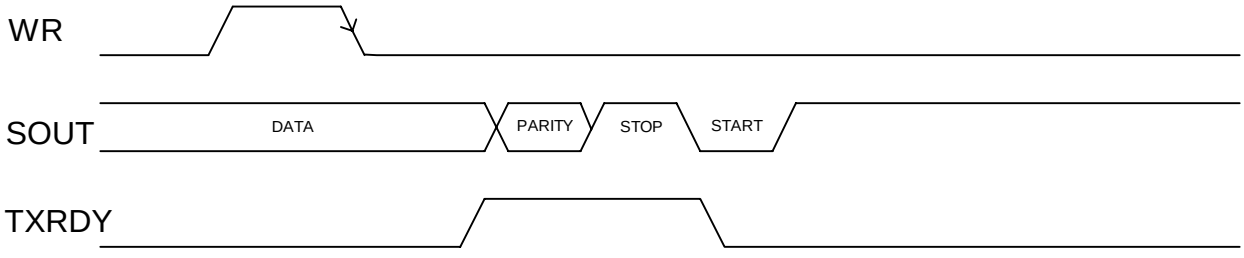
Register Read

The Address (A) and Chip Select (CS) signals are not latched and therefore must be valid throughout the read process. The RD signal is active 1.



Write to Transmitter

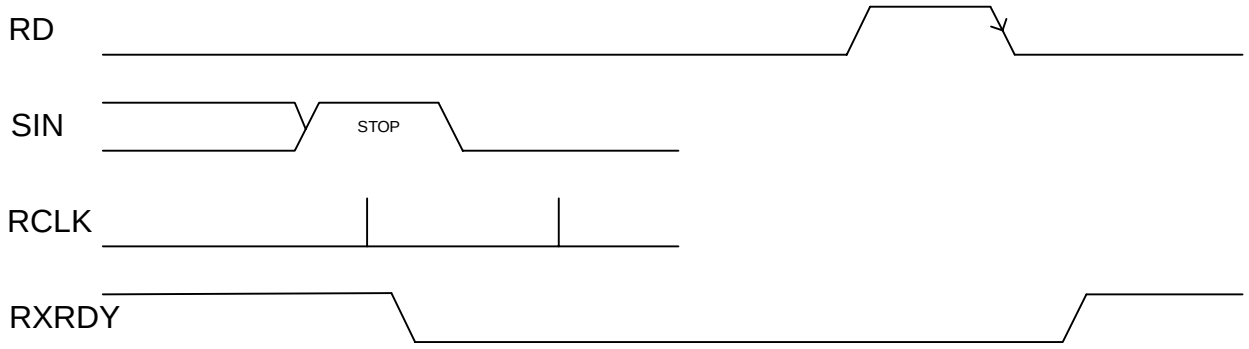
The timing diagram below depicts the situation where the transmitter is in the process of transmitting a byte which is made up of the Data, Parity and Stop bits. Once the byte is written into the Transmitter Holding Register, the TXRDY signal goes into the off (or high) state. This means that the transmitter is ready for a transfer. As the byte just written starts the transmission (with the Start bit) the TXRDY bit goes low showing that the transmitter is ready for the next byte.



Timing Information for Write Function

Read from Receiver

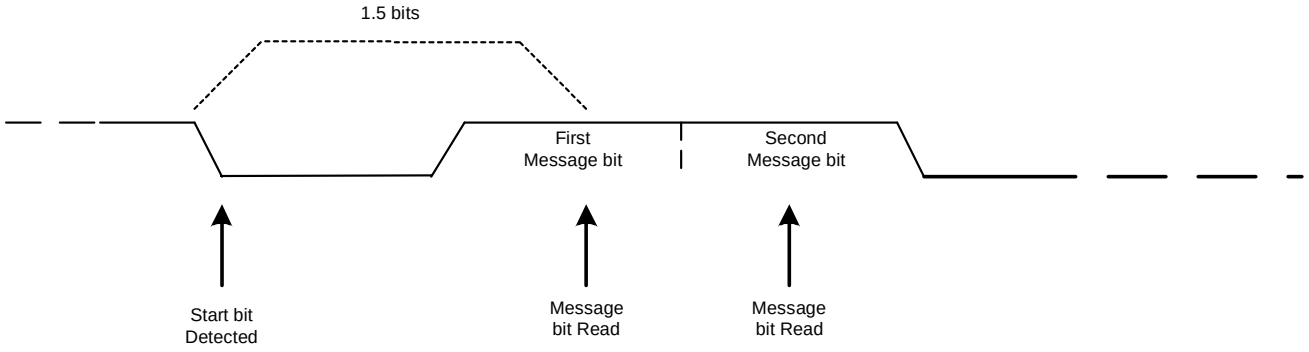
The timing diagram that follows depicts the situation where the receiver is in the process of receiving a byte which is just coming up to the Stop bit. Once a proper Stop bit is received the Byte is placed in the Receiver Buffer Register. This event is signaled to the processor by the RXRDY signal which goes inactive when a byte is awaiting reading. The Receiver Buffer Register must be read before the next byte is received or else an error will be generated.



Timing information for Read Function

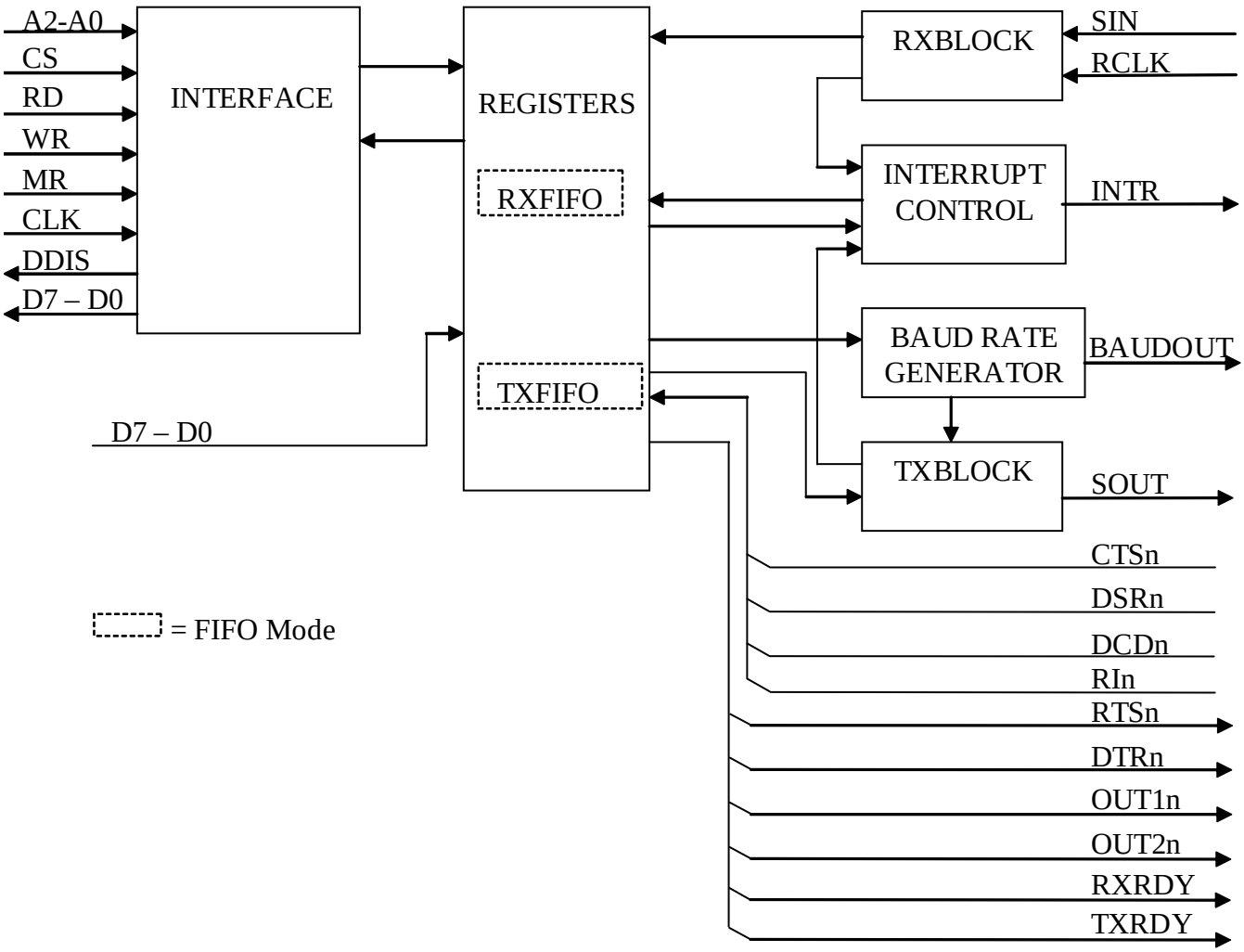
Receiver Synchronization

When the Receiver detects a low state in the incoming data stream it will synchronize to it. After this start edge the UART will wait 1.5*(the normal bit length). This causes the subsequent bits to be read at the middle of its width. This figure depicts this synchronization process.



Receiver Synchronization

Block Diagram



Functional Description

As shown above and explained below, the H8250 includes six major blocks: Interface, Registers, RXBlock, Interrupt Control, Baud Rate Generator, and TXBlock.

Interface

The Interface block is responsible for handling the communications with the processor (or parallel) side of the system. All writing and reading of internal registers is accomplished through this block.

Registers

The Registers block holds all of the device's internal registers. See the Register Description table for details on existing registers and their addresses. Some information comes from the other blocks, but this is all gathered together in the Registers block and made available to all blocks.

RXBlock

This is the receiver block. It handles the receiving of the incoming serial word. It is programmable to recognize data widths such as 5, 6, 7 or 8 bits, various parity settings such as even, odd or no parity and different stop bits of 1, 1½ and 2 bits. It checks for errors in the input data stream such as overrun errors, frame errors, parity errors and break errors. If the incoming word has no problems it is placed in the Receiver Holding register.

Interrupt Control

The Interrupt Control block sends an interrupt signal back to the processor depending on the state of the received and transmitted data. There are various levels of interrupt which can be read from the Interrupt Identification register, which gives the level of interrupt. Interrupts are sent in the condition of empty transmission or receiving buffers, an error in the receiving of a character, or other conditions requiring the attention of the processor.

Baud Rate Generator

This block takes the input clock, CLK, and divides it by a programmed value (from 1 to $2^{16} - 1$). This divided clock is then divided by 16 to create the transmission clock called the Baudout clock. This clock can be connected to the input clock (RCLK) to provide it with a proper clock.

TXBlock

The Transmit block handles the transmission of data written to the Transmission Holding register. It adds required start, parity and stop bits to the data being transmitted so that the receiving device can do the proper error handling and receiving.

Component Substitution

The H8250 megafunction is modeled after the Intel 8250. The following points differentiate the H8250 from the Intel device. In order to create a megafunction with the same functions a wrapper is required. A sample wrapper is included.

- No provision is made for a crystal. The CLK input is designed to accept a standard digital input.
- The bi-directional Data Bus has been split into an input and an output component. In order to use the megafunction with a bi-directional Data Bus, the DDIS signal can be used as the controlling signal for the tri-state drivers.
- RD2, WR2, CS1 and CS2 have been eliminated. A single signal takes their place. These are RD, WR and CS.
- The ADSN signal has been removed. The H8250 functions as if the ADSN signal is held low. The included wrapper can be used to add the ADSN functionality latching the address and data buses.
- The main clock input CLK must be active from power-up.
- The Baudrate Generator is reset to the 0001h value upon activation of the MR signal. Programming the BRG to 0000h is an illegal value. The minimum value for the BRG is 0001h. The Output Data Bus always shows the value of the last register read.

Device Utilization & Performance

Target Device	Speed Grade	Utilization			Performance F_{max}
		LCs	EABs/ESBs	EAB/ESB(bits)	
EPF10K30E	-1	405	0	0	126 MHz
EP20K30E	-1	403	0	0	136 MHz
EP1K10	-1	405	0	0	125 MHz

Deliverables

Netlist License

- AHDL or EDIF netlist
- Assignment & Configuration
- Symbol file
- Include file
- Vectors for testing the functionality of the megafunction including expected results
- Documentation

HDL Source License

- VHDL or Verilog RTL source code
- Testbenches (self checking)
- Wrapper for pin compatible replacement
- Vectors for testing functionality
- Synthesis and simulation scripts
- Documentation

Megafunction Modifications

The H8250 megafunction can be customized to include:

- Removing various control interface signals

Please contact CAST for any required modifications

Contact Information

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